TMDXEVM6678L EVM Known issues

1. Software and Firmware Version List

2. TMDXEVM6678L EVM Design Enhancements

3. TMDXEVM6678L EVM Schematic Corrections

4. TMDXEVM6678L EVM Design Improvements for production

1. Software and Firmware Version List

The PCB version on Beta1 and Beta2 shipments of the TMDXEVM6678L EVM is A101-1 and the PCB number is 19C2830100.
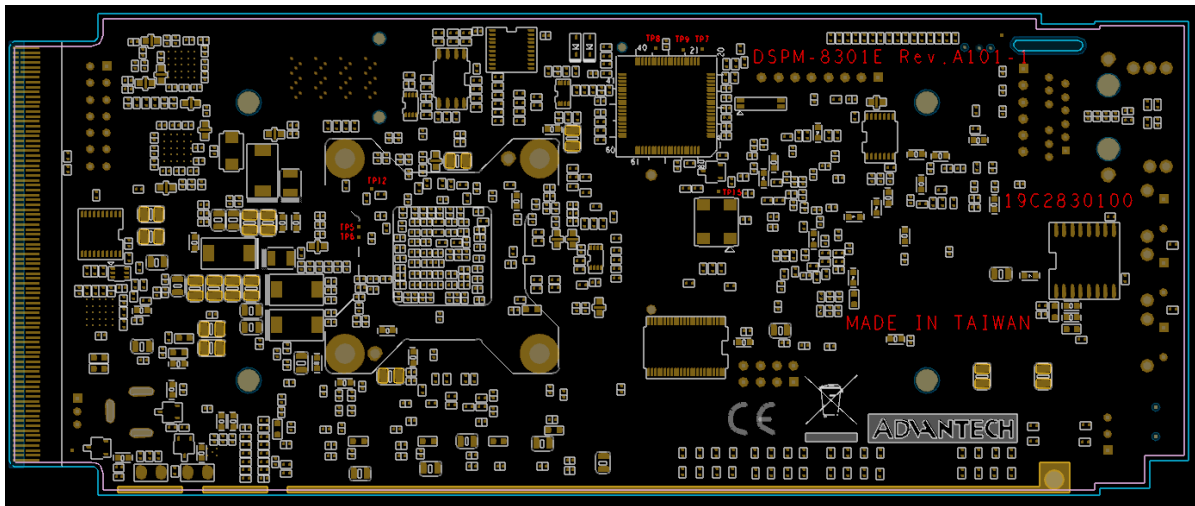
The CCS version on the DVD is 5.0.2.   The MCDSK version on the DVD is 2.0.0.4.   These versions are the same for Beta1 and Beta2 shipments.

The Firmware versions on Beta1 and Beta2 EVMs are shown as the table below.

Item	Beta1	Beta2
UCD9222 (Firmware)	6.2.0	6.4.0
UCD9222 (Configuration file)	UCD9222-48 6.2.0.12575 Address 78 Data Flash.xml	UCD9222 Shannon EVM Project 31Mar11 ver4.xml
FPGA code	Rev.8 (0x08h)	Rev.10 (0x0Ah)
MMC	mmc430_20110301	mmc430_20110301

The Software versions on Beta1 and Beta2 EVMs are shown as the table below.

| Item	Beta1	Beta2
IBL (EEPROM, 0x51h)	1.0.0.1 (?)	1.0.0.2 (?, fix DDR3 issue)
POST (EEPROM, 0x50h)	1.0.0.1	1.0.0.1
NOR flash (SPI)	NA	NA
NAND flash (EMIF-16)	NA	NA

2. TMDXEVM6678L EVM Design Enhancements

2.1 Unexpected EVM Reset Event on the Beta1 EVMs

All Beta1 EVMs have a design erratum that may need to be corrected. The TDI input to the FPGA is floating. This has been observed to allow unexpected FPGA behavior on a small percentage of the boards. Often, the SYSPG_D1 LED goes out and CCS unexpectedly disconnects. A pull-up resistor needs to be added to prevent this from happening. This can be added on the bottom of connector TAP_FPGA1 between pins 1 and 5. Any resistor value between 1K and 10K will suffice. The following figure shows this rework.

Back of the board

TAP_FPGA1
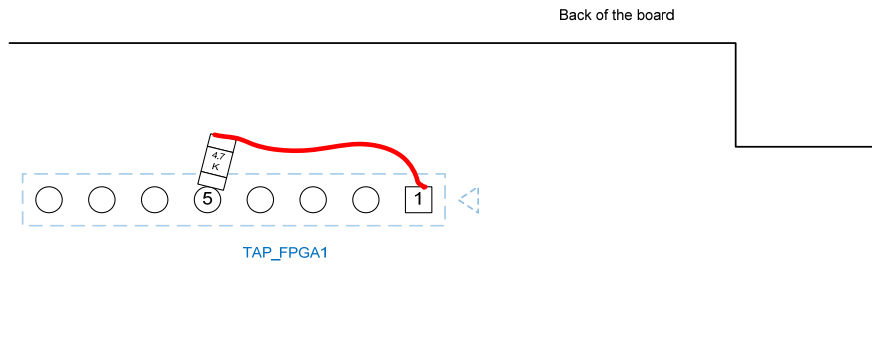
2.2 Incorrect pin out on the HyperLink1 connector on The EVMs

All Beta1 EVMs had populated the iPass+HD mini-SAS connector on the HyperLink1 for the HyperLink connection. The pin out on the HyperLink1 is incorrect, most signals will be shorted if connecting the HyperLink interface by the cable. The HyperLink1 can NOT be used and is not installed on Beta1 and Beta2 EVMs.
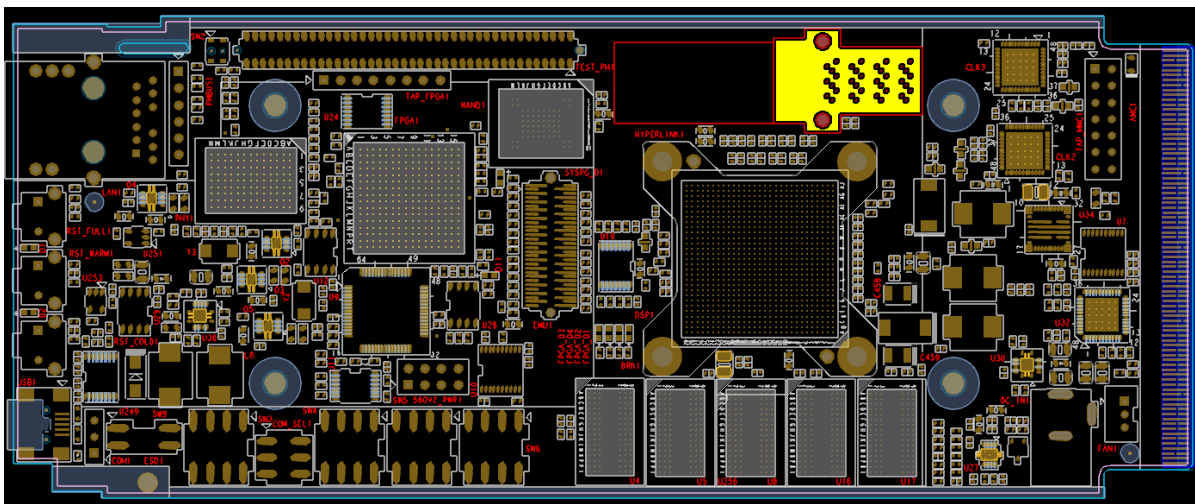
2.3 No HCSL support of the PCIE-CLK from the AMC FCLK on the EVMs

The PCIe clock circuitry does not support HCSL clock from AMC FCLK on Beta1 and Beta2 EVMs. Do NOT try to install the DC-blocking to provide a PCIe clock from the AMC edge connector.

2.4 The CVDD (AVS) power solution on the TMDXEVM6678L EVM

The current CVDD design is limited to 10A maximum.   Operation of the TMS320C6678 at extended temperatures (up to 100C case) and at higher speeds (such as 1.25GHz) may require more than 10A.   Customer designs that require the TMS320C6678 to operate at these performance levels should implement a 15A using the UCD74110.

2.5 The Smart-Reflex® Function on the EVMs

Beta1 EVMs operate the CVDD at a fixed voltage and do not use Smart Reflex.   A new UCD9222 configuration is needed to enable this.   Beta2 EVMs support Smart Reflex. Version 4 of the UCD9222 configuration dated 31MAR must be loaded along with the UCD9222-48_6.3.9.12680 or later firmware.   Version 4 of the UCD9222 configuration must not be loaded until after Version 10 (0xA) of the FPGA is loaded.

Note that Beta1 EVMs can continue being used with a fixed voltage without loss of functionality.

2.6 The FPGA code update issue on the EVMs

The FPGA cannot be reprogrammed while the UCD9222 contains a configuration and it is operating.   One solution requires erasing the configuration from the UCD9222 before programming the FPGA.   The alternate and preferred solution is reprogramming the FPGA from the DSP with CCS connected.   A utility to perform this is available.

Webpage link and file name.

3. The TMDXEVM6678L EVM Schematic Corrections

Changes to the design reflected in Beta1 and Beta2 EVMs

The following changes have been implemented in Beta1 and Beta2 of the TMDXEVM6678L EVM design since the preliminary schematic released December 8, 2010

1) Correction items in the preliminary schematic:
   a) MMC (MSP430) always enabled when power is applied: remove R11, populate R16.
   b) DDR3 slew rate setting set to FAST: remove R72, populate R70.
   c) VCC5_AUX held in off state until enabled by FPGA: remove R237.
   d) I2C SEEPROM changed to STMicro_M24M01-HRMN6TP so that it responded at addresses 50h and 51h as needed
   e) RSV08 connected to GND and RSV09 open: remove R235, populate R234.
   f) 3-pin header for RS-232 changed to contain locking clip.
   g) NAND FLASH changed to Numonyx NAND512R3A2DZA6E.
2) Change DSP clocking input rates to simplify development: CORECLK = PASSCLK = PCIECLK = 100MHz

研華股份有限公司
Advantech Co., Ltd.

台北市內湖區瑞光路26巷20弄1號
No.1, Alley 20, Lane 26, Rueiguang Road
Neihu, District, Taipei, Taiwan 114, R.O.C.
Tel: 886-2-2792-7818 Fax: 886-2-2794-7301
www.advantech.com

4. TMDXEVM6678L EVM Design Improvements for production

Due to some design deficiencies found on Beta version, this section describes the improvements on the production version.

4.1 The UCD9222 and the UCD7242 design for the CVDD (AVS) power supply

1) Remove UCD9222 from FPGA JTAG chain to simplify this circuitry since the UCD9222 does not support boundary scan.
2) Add pull-up resistor to PMBus_CTL as this signal being low prevents the FPGA from sequencing the CVDD and CVDD1 supplies.
3) Correct power supply layout around UCD7242 to comply with datasheet recommendations.   Also increased copper thickness on all plane layers.

Note that the current CVDD design is limited to 10A maximum.   Operation of the C6678 at extended temperatures (up to 100C case) and at higher speeds (such as 1.25GHz) may require more than 10A.   Customer designs that require the C6678 to operate at these performance levels should implement a 15A using the UCD74110.

4.2 The PCB routing of DDR3 on the TMDXEVM6678L EVM

DDR3 layout improvements to meet all guidelines stated in JEDEC UDIMM specification.

4.3 The HCSL support of the PCIE reference clock

Add a buffer and selection method so that an FCLK from the AMC connector in the HCSL format can be used for PCIECLK as well as allowing the existing clock source to be selected.

4.4 Other Changes

1) Add pull-up resistors to the GPIO[15:1] pins and a pull-down resistor to GPIO[0] to keep them from floating after the FPGA stops driving them.

2) Add pull-up resistor to FPGA TDI signal for fixing the power failure issue by unknown reason in the FPGA.

3) Replace MSP430 14-pin JTAG header with 4-pin Spy-Bi-Wire interface to recover board space for power supply layout improvements.

4) Add series termination resistors at HyperLink sideband clock output pins.

5) Correct footprint pin numbering of the HyperLink connector (PCB decal change only).

6) Add circuitry so that JTAG emulation can also be driven from the AMC connector.